AMENDMENTS TO THE SPECIFICATION

Please amend the specification as shown below.

Please amend the paragraph beginning on page 20, line 9, and continuing on page 21, with the following amended paragraph:

First, the sampling must be carried out at three points at the minimum for a half cycle. Sampling of two points gives the rectangular wave itself, so is meaningless. As shown in FIG. 8, in sampling three points, there are two options of the sampling. [Asampling] A sampling 3A (white circles) can be realized by just one ternary-value output switch circuit since it is sufficient to output a, 0, and –a. On the other hand, when a sampling 3B (black circles) is selected, quarterly-values not including 0 are necessary. Therefore, as shown in FIG. 11B and FIG. 11C, two circuits, that is, a binary-value output switch circuit and ternary-value output switch circuit, are required. Note that the half cycle section shown in FIG. 11A is a half open section, therefore, one of the maximum value and the maximum value belongs to the neighboring half cycle section and accordingly in the case of this sampling 3B as well, there are three sampling points in the half cycle.

Please amend the paragraph beginning on page 34, line 17, with the following amended paragraph:

FIG. 21 shows an embodiment thereof. This circuit equivalently realizes inductance by capacitance by using two Gm circuits and therefore is referred to as the "gyrator type" or is

configured by the transmission conductance Gm and the capacitance C so is also referred to as a "Gm-C filter".

Please amend the paragraph beginning on page 39, line 11, and continuing on page 40, with the following amended paragraph:

The pseudo sine wave generated in this embodiment is applied to the inverted input terminal "-" of the operation amplifier 31A as a virtual ground, therefore is input not as the voltage, but as the pseudo sine wave current Ii of the frequency f. Ii passes through the band pass filter 30 and becomes the output Vo. The output Vo is input to a latched comparator 33 and compared with the signal Vref acting as the reference clock used also in the pulse generation circuit 2. The reference signal Vref has the same frequency as Ii and has the same phase. Further, in the band pass filter 30, if the center frequency is equal to the signal frequency, the phases of the input and the output are the same, if the center frequency is lower than the signal frequency, the phase lags, and if the center frequency is higher than the signal frequency, the phase is advanced. The latched comparator 33 outputs "H" when the output Vo is positive at the rising of the pulse of the reference signal Vref, [while] and outputs "L" when it is negative. The center frequency of the band pass filter 30 can be changed by changing the values of one or both of the capacitances C1 and C2 and the resistors R1 and R3 composing the same. In this embodiment, the successive comparison control circuit 34 judges the phases of the voltage Vo and the reference signal Vref. By relatively changing the capacitance or resistance or both one after another, control is carried out so as to obtain the desired center frequency. The successive comparison outputs are supplied to also the slave filter. By keeping a predetermined ratio with

the CR value of the master filter, the filter characteristic of the slave filter also becomes the desired one.